We Claim:

1. A method of interfacing for packet and cell transfer between a first layer device device and a second layer device, comprising:

(a) dividing control information into an in-band portion and an out-of-band portion;

(b) transmitting the in-band portion together with data in a data path from one of said first and said second layer devices to another of said first and said second layer devices; and

(c) transmitting the out-of-band portion outside of the data path from said another of said first and said second layer devices to said one of said first and said second layer devices.

2. A method according to claim 1, wherein said in-band portion is transfer specific information and said out-of-band information is FIFO status flow control information whereby said interface operates independently in both transmit and receive directions.

3. A method according to claim 2, including using a "1 1" framing pattern on a FIFO status channel to mark boundaries of the framing pattern without requiring an out-of-band framing signal.

4. A method according to claim 1, including sending a training control pattern sufficiently often in order to allow a receive interface to check and correct for de-skew on start-up and during regular operation to compensate for skew variations due to changes in voltage, temperature, noise and other factors.

5. A method according to claim 1, including using a FIFO status channel clock transmitted in a direction opposite to data along said data path as a reference source for a data path clock transmitting from a side of an interface between said first and said second layer device opposite to a transmitting end of the FIFO status channel clock.

6. A method according to claim 1, including using a data path clock as a reference source for a FIFO status channel clock transmitting from a side of an interface between said first and said second layer devices opposite to a transmitting end of data along said data path.

7. A method according to claim 4, wherein a transmitting end of the data path sends data and control signals precisely aligned with respect to a source-synchronous clock and the training pattern once every MAX_T where MAX_T is configurable on start-up.

8. A method according to claim 1, wherein each control word contains an error-detection code and one or more control words are inserted between bounded transfer periods whereby performance of the code is not degraded by overly long transfers.

9. A method according to claim 1, wherein an end-of-packet event and error codes are combined into a two-bit code to reduce the number of bits required.

10. A method according to claim 1, wherein transfer information referring to a previous transfer and to a next transfer is contained in one control word.

11. A method of interfacing for packet and cell transfer between a link layer device and a physical layer device (PHY), comprising:

(a) dividing control information into an in-band portion and an out-of-band portion;

(b) transmitting the in-band portion together with data in a data path from one of said link layer device and said PHY to another of said link layer device and said PHY; and

(c) transmitting the out-of-band portion outside of the data path from said another of said link layer device and said PHY to said one of said link layer device and said PHY.

12. A method according to claim 11, wherein said link layer device has a transmit link layer device operative to transmit data from said transmit link layer device to said PHY and a receive link layer device operative to transmit data from said PHY to said receive link layer device.

13. A method according to claim 11, wherein said in-band portion includes packet address, delineation and error control coding and said out-of-band information is FIFO status flow control information whereby said interface operates independently in both transmit and receive directions.

14. A deskewing circuit for deskewing data arriving on a plurality of data lines, comprising:

(a) a plurality of serial-in parallel out (SIPO) blocks coupled to said plurality of data lines operative to convert serial input data from a corresponding respective plurality of data lines to parallel data;

(b) a plurality of registers coupled to said SIPO blocks, said registers operative to store successive words of data arriving on said data lines with one word stored on each of said registers;

(c) a training detector block coupled to said registers and operative to detect the presence of a training pattern based on the contents of said registers;

(d) a plurality of transition detection blocks coupled to said registers and operative to search and to detect a transition in each bit position of said registers;

(e) an aligner block coupled to said transition detection blocks operative to select an appropriate register from which to read each bit in order to present a deskewed output.

15. A deskewing circuit, comprising:

(a) 17 serial-in parallel-out (SIPO) blocks, each one coupled to a corresponding input data line and operative to convert serial input data to parallel output data, each of said SIPO blocks having N outputs where N is an integer equal to a word size of data output from each of said SIPO blocks, each of said SIPO blocks having separate bit outputs for each bit of a word converted by said each of said SIPO blocks;

(b) N registers coupled to said separate bit outputs of each of said SIPO blocks such that an i^{th} one of said N registers is connected to an i^{th} bit output of said SIPO blocks, where i=1, 2, .., N;

(c) a training detector block coupled to outputs of said registers operative to detect the presence of a training pattern based on the contents of said registers;

(d) 17 transition detection blocks coupled to outputs of said registers with an i^{th} transition detection block coupled to an i^{th} bit output of each of said registers, where i=1, 2,.., 17, said i^{th} transition detection block, when after the presence of a training pattern has been detected, is operative to search for a transition on an i^{th} bit position from said 17 registers; and

(e) an aligner block coupled to outputs from said 17 transition blocks operative to select an appropriate register from which to read each bit in order to present a deskewed output.